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TITLE

ACTIVE MATRIX DISPLAY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to an LCD circuit and particularly to an active matrix display device using the gate-to-gate signal for light-on test as the common voltage supplied to the storage capacitor.

Description of the Prior Art:

Liquid crystal displays (LCD) have in recent years been substituted for CRTs (Cathode Ray Tubes) as display units. This is mainly because LCDs provide the advantage of occupying less area than CRTs because LCDs are flat display units. Therefore, LCDs require less space and the demand for LCDs as portable and household displays has increased dramatically.

Moreover, LCDs provide the advantage consuming less power than CRTs. In particular, an active-matrix liquid crystal display that mounts an active element for each picture element of a liquid crystal display panel is noteworthy because it provides a display quality equal to that of a CRT.

FIGS. 1 and 2 are a typical schematic and a sectional view showing the structure of an existing TFT-LCD. First, the structure of the existing TFT-LCD is described below by referring to FIG. 1. The TFT-LCD comprising an array substrate 12 on which pixel electrodes 10 are formed in a matrix and a facing substrate 14 arranged so as to face the

array substrate surface at a predetermined interval. A TFT 16 serving as a switching element is formed near the pixel electrodes 10 on the array substrate 12 of the TFT-LCD respectively and source electrodes 18 of these TFTs are connected to the pixel electrodes 10. A gate electrode 20 and a drain electrode 22 of a TFT are connected to the scan signal line 24 and data signal line 26 constituting a row and a column of a matrix respectively. The scan signal lines 24 and the data signal lines 26 are formed at predetermined intervals and they are all perpendicular to each other. Moreover, each pixel electrode 10 has a necessary capacitance between the pixel electrode 10 and the storage capacitance line 28. This capacitance serves as a storage capacitance 29.

As shown in FIG. 2, an existing TFT-LCD has a structure in which an undercoat layer 42, a gate electrode 20 (scan signal line 24), a pixel electrode 10, a gate insulating film 44, a semiconductor layer (channel layer) 46, a channel protective film 48, an ohmic contact layer 50, a passivation film 52, and an alignment film 54 are deposited on an array substrate 12. Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD corresponding to an area in which pixel electrodes 10 on the array substrate 12 are arranged in a matrix. I16ut signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of

these signals, the potential of the common electrode 30 on the facing substrate is supplied from a plurality of portions of electrodes on the array substrate through a transfer 62 using conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electrical resistance, the electrical resistance from a potential supply terminal to the central portion of a display screen increases as a display unit increases in size. Moreover, in the case of a color-display TFT-LCD, a color filter 32 consisting of three primary colors of red (R), green (G), and blue (B) is formed in a matrix between the facing substrate 14 and the common electrode 30 corresponding to the pixel electrode 10 of the array substrate 12. Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing film 38 is frequently set at the outer laterals of the array substrate 12 and the facing substrate 14. Furthermore, a direct-view transmission-type TFT-LCD has a backlight 68 and an image is output by controlling the transmittance of an incident light 69 emitted from the backlight 68.

The finished liquid crystal displays must be tested for quality assurance before leaving the factory. The light-on test is one of the quality tests that should be carried out. Test transistors equal to the number of rows of pixels are formed next to the pixel array and used as switches for the light-on test, as shown in FIG. 3. During the light-on test, a gate-to-gate signal LCDQ1 is raised to a high logic voltage level to turn on the test transistors NL1~NL4, by which gate signals LCDQ2 are transferred through scan signal lines 24 to the gates of the switching transistors 16. Thus, all the switching transistors 16 in the pixel array PA are turned on. In the mean time, data signals DS are provided through data signal lines 26 to illuminate all the pixels. After the light-on test, the gate-to-gate signal LCDQ1 is pulled down to a low logic voltage level to isolate the signals LCDQ2 from the scan signal lines 24.

As shown in FIG. 3, a conducting line CL is also formed next to the pixel array PA to supply a common voltage Vcom to the storage capacitors 29. The conducting line CL must be bold enough to conduct a large current to or from the large number of pixels. There may be also some other elements formed next to the pixel array PA, such as ESD protection devices or patterns for alignment during the process. However, the width of the margin area next to the pixel array PA in the present LCDs may be smaller than 4cm. Dividing the limited space provided for the bold conducting lines CL and LL presents a problem.

SUMMARY OF THE INVENTION

The object of the present invention is to provide an active matrix display device using the gate-to-gate signal for light-on test as the common voltage supplied to the storage capacitor.

The present invention provides An active matrix display device having a display region consisting of sub-pixels arrayed in a matrix fashion, the sub-pixels having switching elements, comprising a plurality of data and scan signal lines, and common voltage lines for sending signals and a reference voltage to the sub-pixels, test transistors, each of which is connected to one of the plurality of scan signal lines for sending test signals thereto, and a plurality of input terminals, each of which is connected to one of a plurality of the test transistors, wherein each gate of the test transistors and each of the common voltage lines are connected to one of the input terminals, the test transistors control inputs of the test signals to the sub-pixels.

The present invention also provides a liquid crystal display panel comprising an array substrate on which an active matrix display device is formed, wherein the active matrix display device comprises a plurality of data and scan signal lines, and common voltage lines for sending signals and a reference voltage to the sub-pixels, test transistors, each of which is connected to one of the plurality of scan signal lines for sending test signals thereto, and a plurality of input terminals, each of which is connected to one of a plurality of the test transistors, wherein each

gate of the test transistors and each of the common voltage lines are connected to one of the input terminals, the test transistors control inputs of the test signals to the sub-pixels, a facing substrate having a common electrode, and a liquid crystal sealed between the array and facing substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, given by way of illustration only and thus not intended to be limitative of the present invention.

FIG. 1 is a perspective view of the structure of a TFT-LCD.

Fig. 2 is a sectional view of the structure of the TFT-LCD, taken along the line AA of FIG. 1.

FIG. 3 is a schematic diagram showing a conventional LCD circuit.

FIG. 4 is a schematic diagram showing an LCD circuit according to one embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 and 2 are a schematic and a sectional view showing the structure of a TFT-LCD according to one embodiment of the invention. As shown in FIG. 1, the TFT-LCD includes an array substrate 12 on which pixel electrodes 10 are formed in a matrix and a facing substrate 14 arranged so as to face the array substrate surface at a predetermined interval. A TFT 16 serving as a switching element is formed near the pixel electrodes 10 on the array substrate 12 of the TFT-LCD respectively and source electrodes 18 of these

TFTs are connected to the pixel electrodes 10. A gate electrode 20 and a drain electrode 22 of a TFT are connected to the scan signal line 24 and data signal line 26 for receiving scan signals SS and data signals DS from the scan driver SD and data driver DD constituting a row and a column of a matrix respectively. The scan signal lines 24 and the data signal lines 26 are formed at predetermined intervals and they are all perpendicular to each other. Moreover, each pixel electrode 10 has a necessary capacitance between the pixel electrode 10 and the storage capacitance line 28. This capacitance serves as a storage capacitance 29.

As shown in FIG. 2, an existing TFT-LCD has a structure in which an undercoat layer 42, a gate electrode 20 (scan signal line 24), a pixel electrode 10, a gate insulating film 44, a semiconductor layer (channel layer) 46, a channel protective film 48, an ohmic contact layer 50, a passivation film 52, and an alignment film 54 are deposited on an array substrate 12. Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD corresponding to an area in which pixel electrodes 10 on the array substrate 12 are arranged in a matrix. I16ut signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of these signals, the potential of the common electrode 30 on the facing substrate is supplied from a plurality of portions of electrodes on the array substrate

through a transfer 62 using conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electrical resistance, the electrical resistance from a potential supply terminal to the central portion of a display screen increases as a display unit increases in size. Moreover, in the case of a color-display TFT-LCD, a color filter 32 consisting of three primary colors of red (R), green (G), and blue (B) is formed in a matrix between the facing substrate 14 and the common electrode 30 corresponding to the pixel electrode 10 of the array substrate 12. Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing film 38 is frequently set at the outer laterals of the array substrate 12 and the facing substrate 14. Furthermore, a direct-view transmission-type TFT-LCD has a backlight 68 and an image is output by controlling the transmittance of an incident light 69 emitted from the backlight 68.

FIG. 4 shows the LCD circuit on the array substrate 12. Test transistors NL1~NL4 equal to the number of rows of pixels are formed next to the pixel array PA on the array substrate 12 and used as switches for the light-on test.

The test transistors NL1~NL4 have drains/sources coupled to the scan signal lines 24, sources/drains coupled to receive a LCDQ2 signal and gates coupled to receive a LCDQ1 signal. The test transistors NL1~NL4 are turned on by the signal LCDQ1 so that the signals LCDQ2 are transmitted on the scan signal lines 24 to illuminate the pixels during the light-on test. The transistors NL1~NL4 are turned off by the signal LCDQ1 so that the signals LCDQ2 isolated from the scan signal lines 24 and the signal LCDQ1 is used as the common voltage Vcom supplied to the storage capacitors 29 in the pixels through the storage capacitance lines 28 beyond the light-on test.

By comparing the LCD circuits shown in FIG. 3 and 4, it is noted that the circuit in FIG. 4 has only one conducting line formed next to the pixel array PA. The low logic voltage level of the signal LCDQ1 beyond the light-on test is used as the common voltage Vcom.

Alternatively, the test transistors NL1~NL4 may have drains/sources coupled to the data signal lines 26 instead of the scan signal lines 24, or, in addition to the test transistors NL1~NL4, there may be test transistors having drains/sources coupled to the data signal lines 26. Further, this circuit configuration is suitable for a normally white pixel array. The common voltage is provided by the LCDQ signal which is different from the voltage on the common electrode of the facing substrate. By shorting the switching transistor to the common voltage line to bypass the storage capacitor, the voltage difference between the common electrodes of the array and facing substrate turns a defect pixel to a dark pixel. Thus, there is no

white pixel even if there are defects in a normally white pixel array.

In conclusion, in the present invention, the storage capacitance lines of the pixels are directly coupled to the conducting line for the signal LCDQ1. The low logic voltage level of the signal LCDQ1 beyond the light-on test is used as the common voltage supplied to the storage capacitor. There is only one bold conducting line formed in the limited margin area next to the pixel array. This eliminates the layout problem in the conventional LCD circuit.

The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. Obvious modifications or variations are possible in light of the above teaching. The embodiments were chosen and described to provide the best illustration of the principles of this invention and its practical application to thereby enable those skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. All such modifications and variations are within the scope of the present invention as determined by the appended claims when interpreted in accordance with the breadth to which they are fairly, legally, and equitably entitled.